Bipolar Junction Transistor (BJT)

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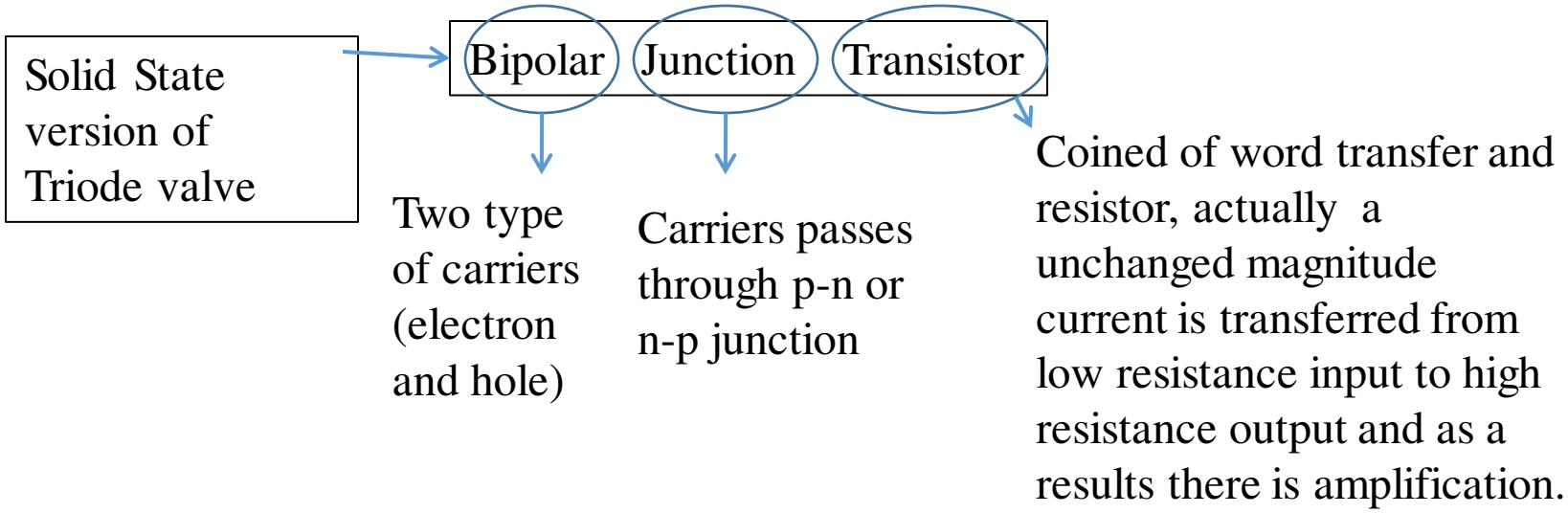
Introduction and History



- One of the most important invention in electronics of 20th Century.
- Walter H Brattain and John Bardeen demonstrated point contact transistor in Dec'1947
- William Shockley made theoretical invention in Jan'1948
- Finally junction transistor appeared in 1950.

Structure

Junction Transistor is made up of semiconductor (Ge or Si)

N-type thin layer is sandwiched between two P-type layer.

P-type thin layer is sandwiched between two N-type layer.

Emitter
The left hand section of each transistor is called emitter. It is heavily doped compared to other regions. Its main function to supply majority carriers.

Base
Middle Section of transistor. It is very thin and very lightly doped.

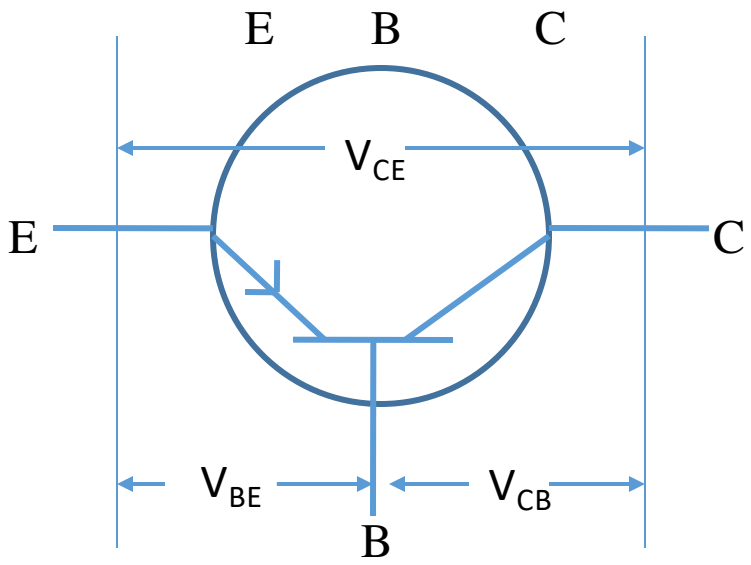
Collector
The right hand section of each transistor is called Collector. Its doping is intermediate of emitter and base. But physical structure is larger than others because it has to dissipate much greater power.

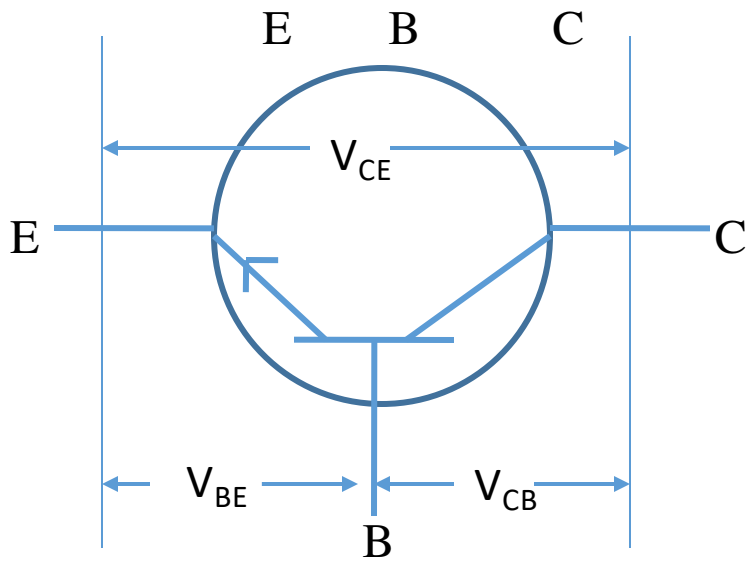
Emitter Junction

Collector Junction

Then, is it possible to invert the transistor?

Circuit Symbols

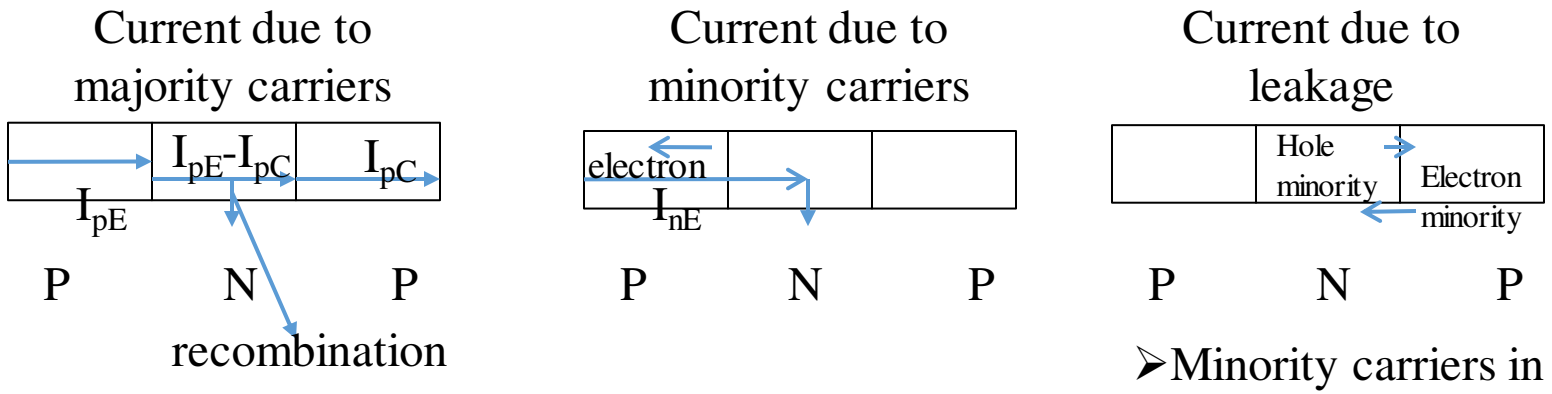


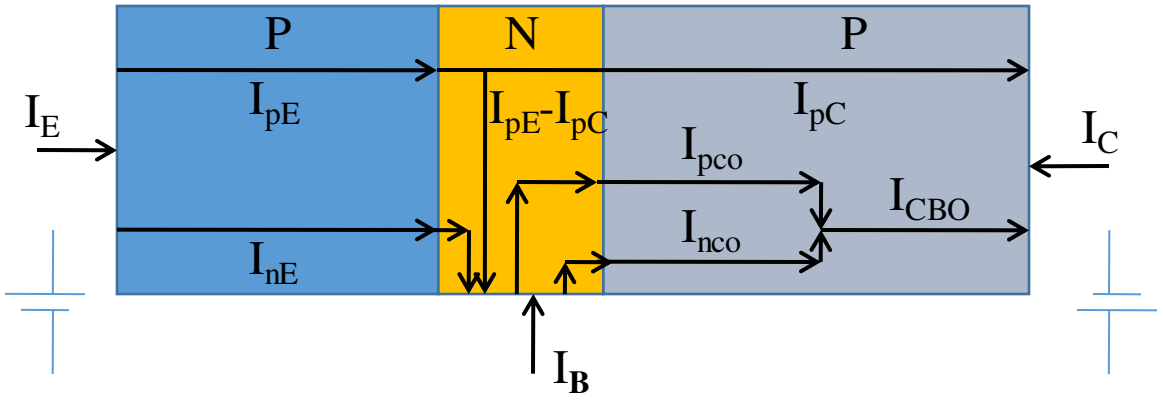


- Arrow is given on emitter as it supply carriers.
- Arrow direction is given in conventional current direction.

Current Component in Transistor

- In BJT there are two types of carriers Electrons and Holes.
- In PNP, Holes are Majority Carriers and electrons are Minority Carriers.
- For normal functioning the emitter junction should be in forward bias and collector junction should be in reverse bias.
- There are three types of current in transistors:





- Minority carriers in base and in collector are in forward bias.
- These are generated due to thermal energy. So, they flow even when emitter is disconnected.
- This is temperature dependent.

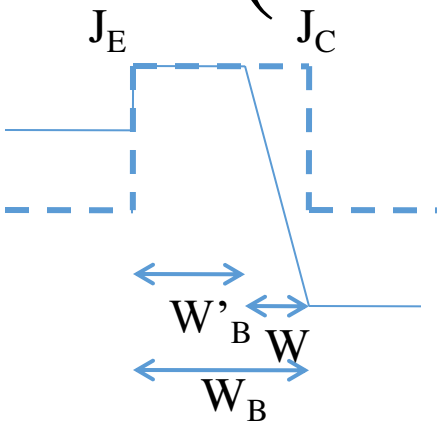
Thus sign of current and voltage are,

Transistor Type	I_E	I_B	I_C	V_{EB}	V_{CB}	V_{CE}
P-N-P	+	-	-	+	-	-
N-P-N	-	+	+	-	+	+

So, total collector current , $I_C=I_{pC}+I_{CO}=\alpha I_E+I_{CO}$
Here, α is the fraction of total emitter current collected by the collector. Since, in PNP, I_E is +ve and I_C and I_{CO} are –ve. So, $\alpha=-(I_C - I_{CO})/I_E$
Here, α is called large signal current gain in CB configuration. (I_E is input and I_C is output)

In CE configuration, I_B is input and I_C is output.
We have, $\alpha=-(I_C - I_{CO})/I_E = -(I_C - I_{CO})/-(I_c + I_B)$
therefore, $\alpha(I_c + I_B)=(I_C - I_{CO})$
This gives, $I_C=(\alpha/(1-\alpha))I_B+(1/(1-\alpha))I_{CO}$
$=\beta I_B+(1+\beta)I_{CO}$
$=\beta I_B+I_{CEO}$
Here, β is large signal current gain in CE configuration. And $\beta=\alpha/(1-\alpha)$

Early Effect (Band-width Modulation)



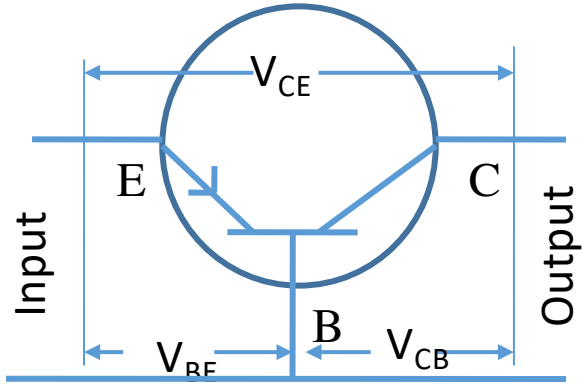
- W changes depending upon reverse bias voltage and doping concentration.
- With increase of reverse bias voltage depletion width increases.
- With increase of doping depletion width decreases.

- Thus with the variation of reverse bias voltage effective width of base varies. This is known as Base width Modulation or in honour of J M Early it is also called Early Effect.

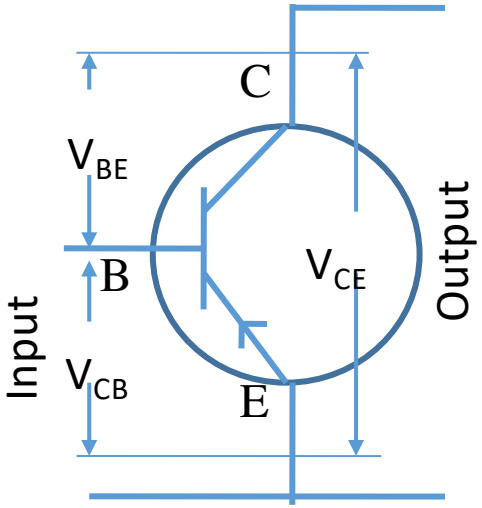
Consequences:

1. With increase of reverse voltage base width decreases, so recombination decreases and collector current increases.
2. As base width decreases the hole concentration gradient increases, so emitter current increases.
3. If the reverse voltage is such that effective width of base become zero then breakdown occur. This phenomena is called reach through or punch through.

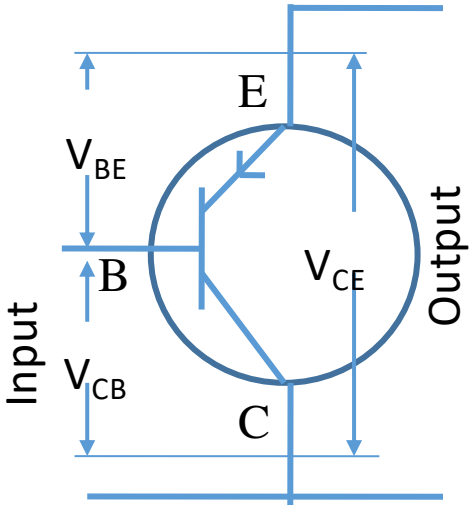
Transistor Configuration



CB-Configuration



CE-Configuration



CC-Configuration

Common Emitter Configuration

In this configuration we use emitter as common terminal for both input and output. This common emitter configuration is an inverting amplifier circuit. Here the input is applied between base-emitter region and the output is taken between collector and emitter terminals.

- input parameters are V_{BE} and I_B
- output parameters are $V_{CE}$and I_C.

This type of configuration is mostly used in the applications of transistor based amplifiers. In this configuration the emitter current is equal to the sum of small base current and the large collector current. i.e. $I_E = I_C + I_B$.

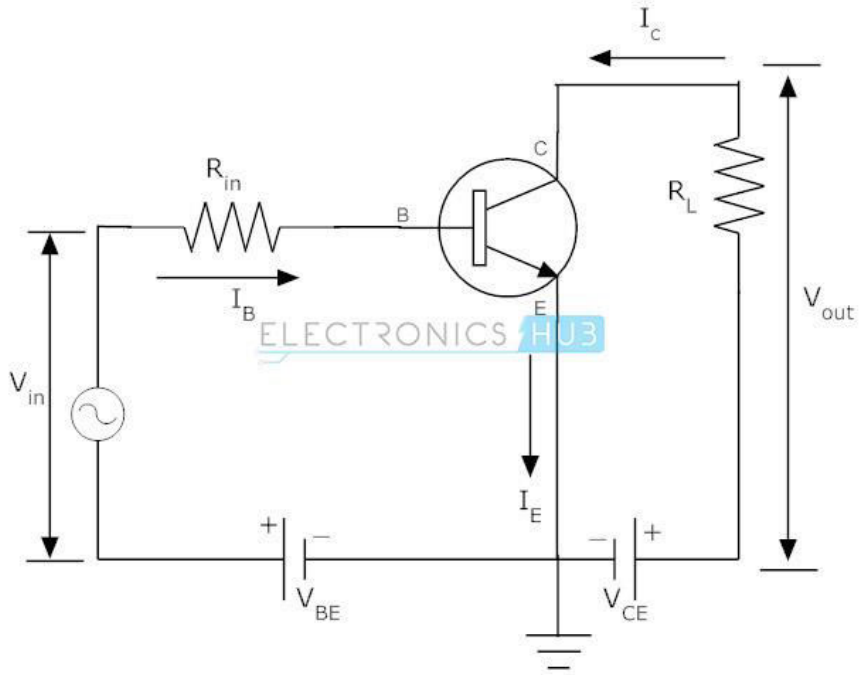
- We know that the ratio between collector current and emitter current gives **current gain alpha** in **Common Base** configuration similarly the ratio between collector current and base current gives the **current gain beta** in **common emitter configuration**.

ADVANTAGEs:

This configuration is mostly used one among all the three configurations.

- It has medium input and output impedance values.
- It also has the medium current and voltage gains.

But the output signal has a phase shift of 180 degree i.e. both the input and output are inverse to each other.



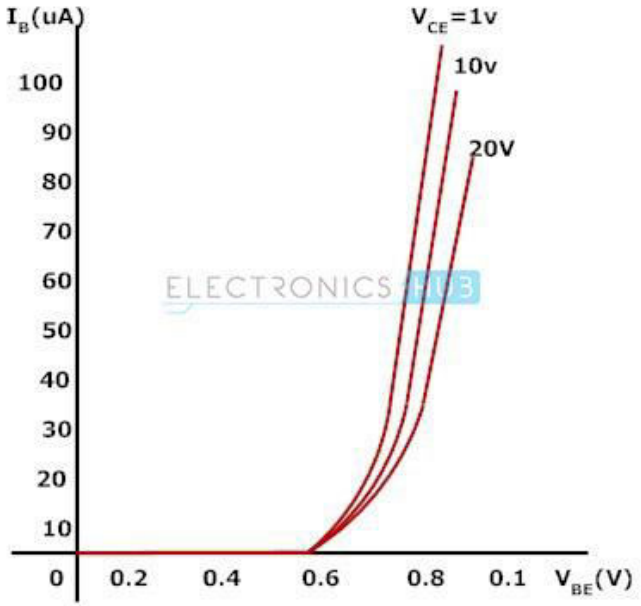
Input Characteristics

The input characteristics of common emitter configuration are obtained between input current I_B and input voltage V_{BE} with constant output voltage V_{CE}. Keep the output voltage V_{CE}constant and vary the input voltage V_{BE} for different points, now record the values of input current at each point. Using these values we need to draw a graph between the values of I_B and V_{BE} at constant V_{CE}. The equation to calculate the input resistance R_{in} is given below.

$R_{in} = V_{BE}/I_B$ (when V_{CE} is at constant)

It is to be noted that ,

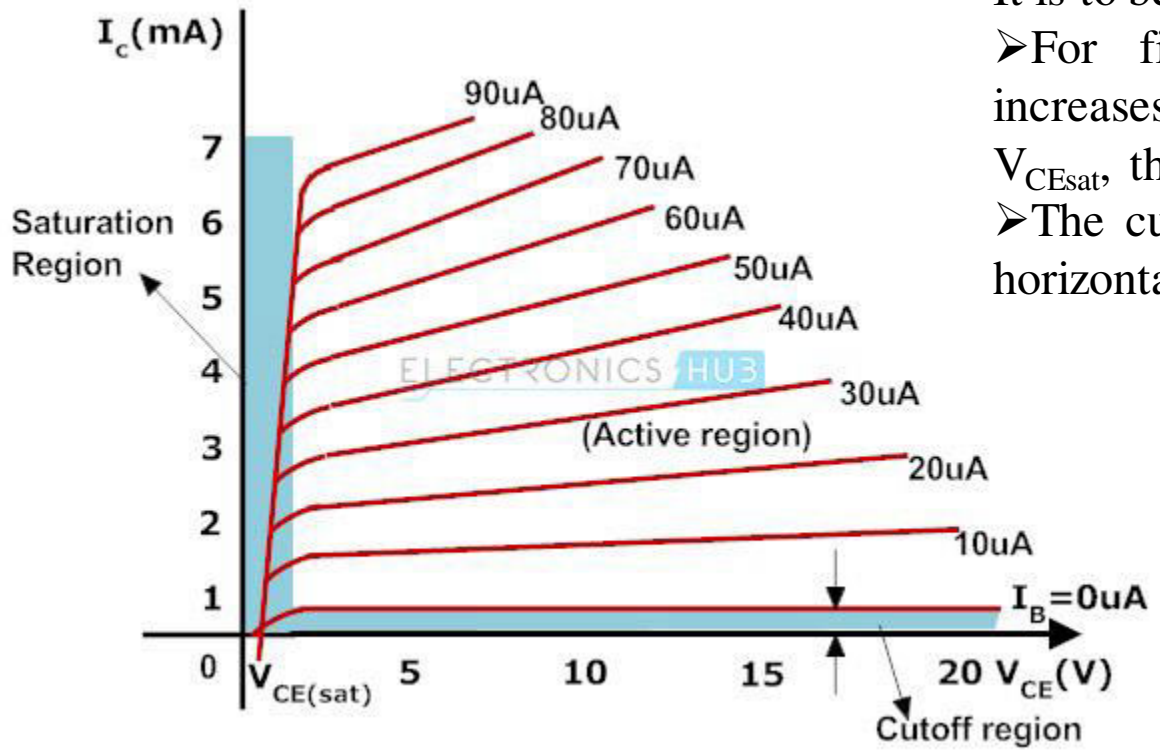
- The input current is in microampere range.
- For a fixed value of V_{CE} input current increases exponentially with V_{BE} after V_{BE} exceeds the cut-in voltage.
- For fixed V_{BE} , I_B decreases as V_{CE} increases. This is because with the increase of output voltage collector junction reverse bias voltage increases which decrease the effective base width. So recombination decreases. Thus the I_B decreases.



Output Characteristics

The output characteristics of common emitter configuration are obtained between the output current I_C and output voltage V_{CE} with constant input current I_B. Keep the base current $I_B$constant and vary the value of output voltage V_{CE} for different points, now note down the value of collector I_C for each point. Plot the graph between the parameters I_C and V_{CE} in order to get the output characteristics of common emitter configuration. The equation to calculate the output resistance from this graph is given below.

$R_{out} = V_{CE}/I_C$ (when I_B is at constant)



It is to be noted that ,

- For fixed I_B the collector current increases rapidly with V_{CE} from zero to V_{CEsat}, then I_C does not vary rapidly.
- The curves at active region are not so horizontal as they are in CB mode.

In active region, $I_E=I_C+I_B$
Again,

Thus we get,

$$I_C = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CO}}{1-\alpha}$$

Let us define,

$$\beta = \frac{\alpha}{1-\alpha}$$

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

Let,

$$(1+\beta) I_{CO} = I_{CEO}$$

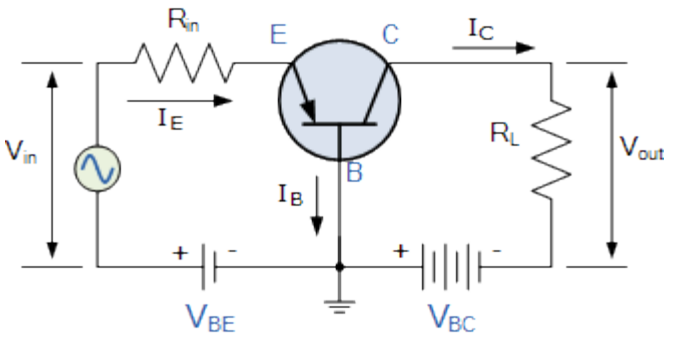
Thus,

$$I_C = \beta I_B + I_{CEO}$$

Here, β is the large signal current gain in CE mode. For typical value $\alpha = 0.99, \beta = 99$
Therefore, slope is higher than CB mode.

Amplifying action of a transistor:

In this amplifier, input signal ΔV_i is connected and a load resistance R_L is connected to the output. As the input current I_E changes exponentially with input voltage, so a small change ΔV_i causes large change in emitter current change ΔI_E .Therefore, the change in collector current is,



$$\Delta I_C = \alpha_{ac} \Delta I_E$$

So change in output voltage is as follows,

$$\Delta V_O = -R_L \Delta I_C = -R_L \alpha_{ac} \Delta I_E$$

So, voltage amplification,

$$A_v = \frac{\Delta V_o}{\Delta V_i} = -\frac{R_L \alpha_{ac} \Delta I_E}{r_e \Delta I_E} = -\frac{R_L \alpha_{ac}}{r_e}$$

r_e is the dynamic resistance of the emitter junction. For example, taking R_L =5kohm and the common values of re= 25 ohm and $\alpha_{ac} = 0.99$, Av=-198 i.e. the output signal is amplified by 198 times.

Thus, amplification action is done by transferring the current from low resistance input to high resistance output circuit.

Relations of Current amplification factor

The ratio of change in collector current to the change in emitter current at constant collector-base voltage is known as current amplification factor.

$$\alpha = \frac{I_C}{I_E}$$

The ratio of change in collector current to the change in base current is known as base current amplification factor.

$$\beta = \frac{I_C}{I_B}$$

$$I_C = \alpha I_E = \beta I_B$$

$$I_E = I_C + I_B$$

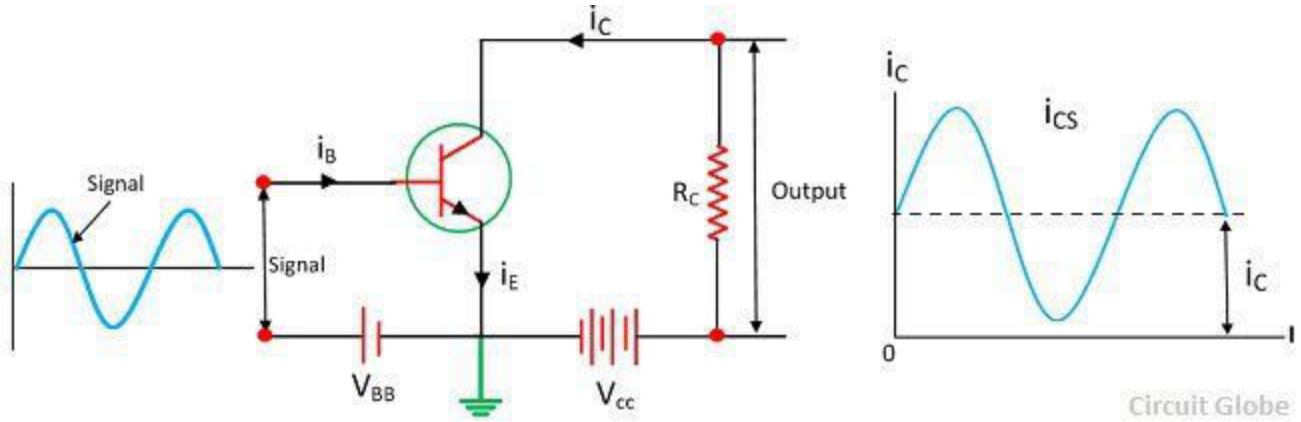
$$\alpha = \frac{\beta}{\beta + 1}$$

$$\beta = \frac{\alpha}{\alpha - 1}$$

End of Lec-1

Application of Transistor

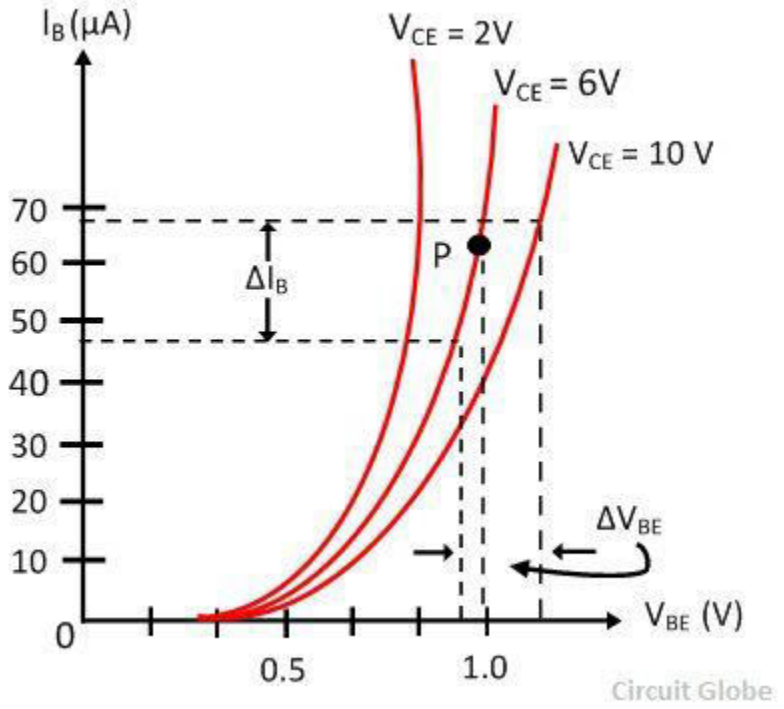
DC Biasing Circuits

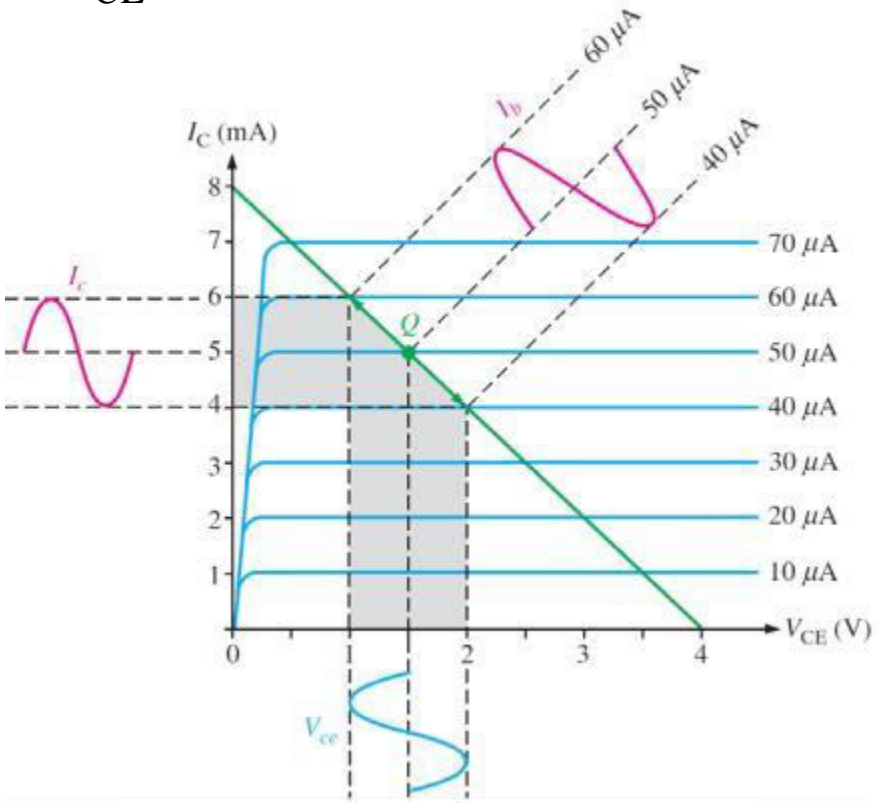


- The **ac** operation of an amplifier depends on the initial **dc** values of I_B, I_C, and V_{CE}.
- By varying I_B around an initial dc value, I_C and V_{CE} are made to vary around their initial dc values.
- **DC** biasing is a static operation since it deals with setting a **fixed (steady)** level of current (through the device) with a desired fixed voltage drop across the device.

Purpose of the DC biasing circuit

- To turn the device “ON”
- To place it in operation in the region of its characteristic where the device operates most linearly, i.e. to set up the initial dc values of I_B, I_C, and V_{CE}





Q point or quiescent or operating point of BJT

- Q-point is an acronym for quiescent point. Q-point is the operating point of the transistor (I_{CQ},V_{CEQ}) at which it is biased.
- To operate the BJT at a point it is necessary to provide voltages and currents through external sources.
- The concept of Q-point is used when transistor act as an amplifying device and hence is operated in active region of input output characteristics.

Importance of Q point in transistor

Normally whatever signals we want to amplify will be of the order millivolts or less. If we directly input these signals to the amplifier they will not get amplified as transistor needs voltages greater than cut in voltages for it to be in active region. Only in active region of operation transistor acts as amplifier. So we can establish appropriate DC voltages and currents through BJT by external sources so that BJT operates in active region and superimpose the AC signals to be amplified. The DC voltage and current are so chosen that the transistor remains in active region for entire AC signal excursion. All the input AC signals variations happen around Q-point.

Q-point is generally taken to be the intersection point of load line with the output characteristics of the transistor. There can be infinite number of intersection points but q-point is selected in such a way that irrespective of AC input signal swing the transistor remain in active region.

Faithful Amplification

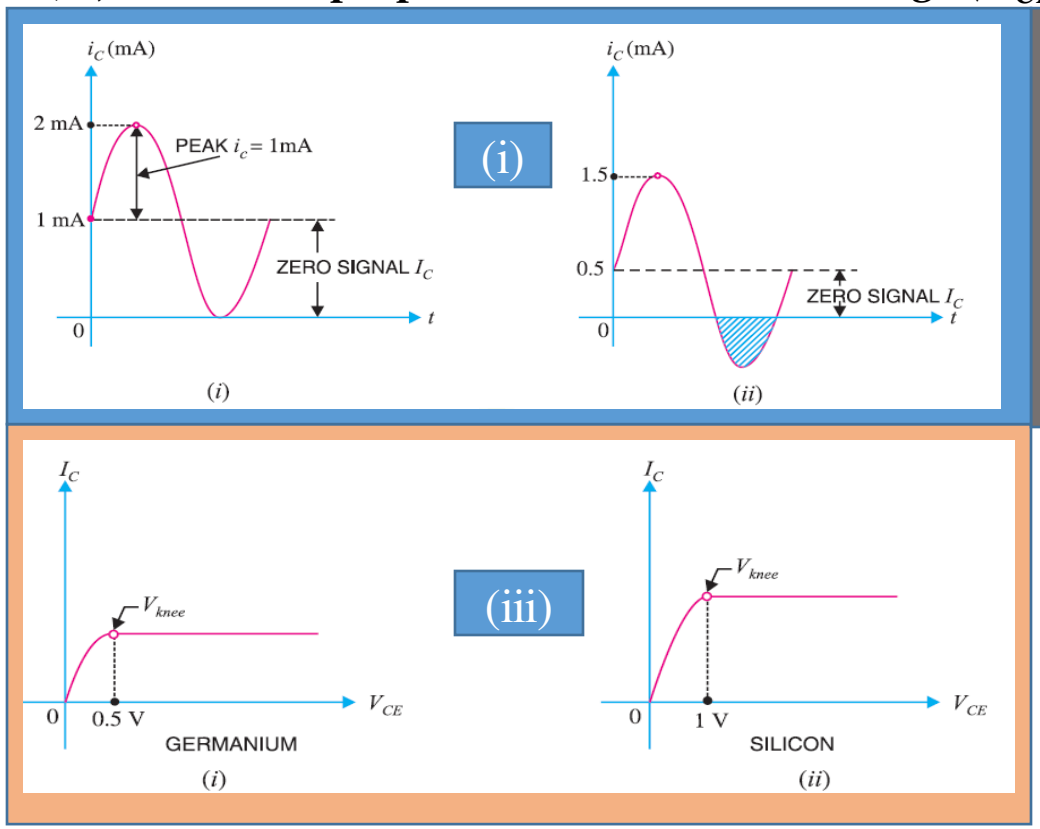
➢*The process of raising the strength of a weak signal without any change in its general shape is known as* ***faithful amplification.***

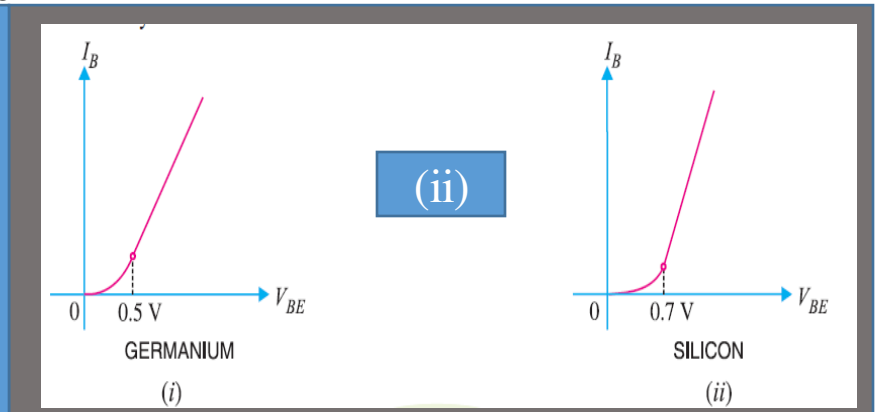
The theory of transistor reveals that it will function properly if its input circuit (*i.e. base-emitter* junction) remains forward biased and output circuit (*i.e. collector-base junction) remains reverse* biased at all times. This is then the key factor for achieving faithful amplification. To ensure this, the following basic conditions must be satisfied :

(i) Proper zero signal collector current

(ii) Minimum proper base-emitter voltage (V_{BE}) at any instant

(iii) Minimum proper collector-emitter voltage (V_{CE}) at any instant





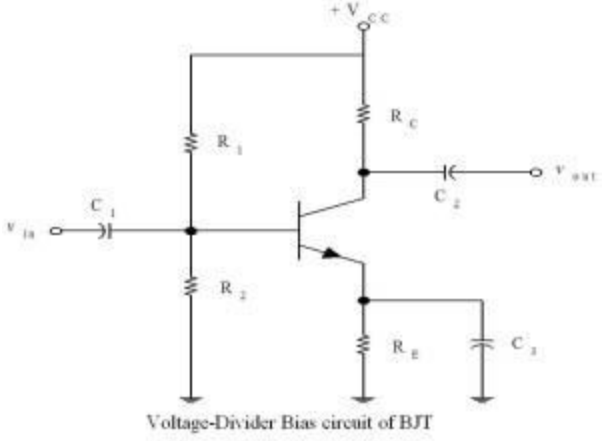
The conditions *(i) and (ii) ensure that base-emitter junction shall remain properly forward biased* during all parts of the signal. On the other hand, condition *(iii) ensures that base-collector junction* shall remain properly reverse biased at all times. In other words, the fulfilment of these conditions will ensure that transistor works over the active region of the output characteristics *i.e. between* saturation to cut off.

DC load line

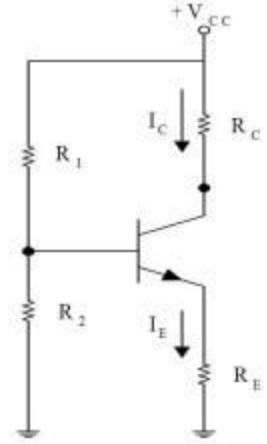
The dc load line is the locus of I_C and V_{CE}at which BJT remains in active region i.e. it represents all the possible combinations of I_C and V_{CE} for a given amplifier.

Procedure to draw DC load line

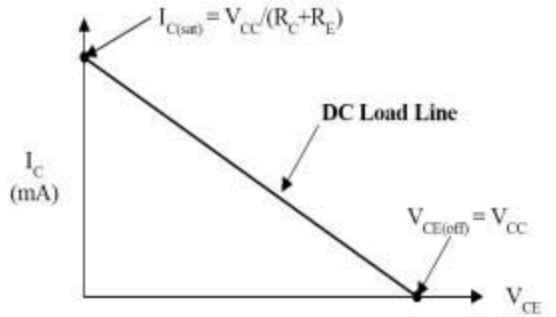
To draw DC load line of a transistor we need the maximum possible current (saturation current) through the transistor and occurs at the point where the voltage across the collector is minimum and the maximum possible voltage across the collector (cutoff voltage) and occurs at zero collector current.



Voltage divider bias circuit of BJT



DC equivalent of Voltage divider bias ciruit of BJT



DC load line

The biasing and blocking capacitors acts as open circuit for DC signals hence can be represented by open circuit terminals. From the DC equivalent circuit by applying KVL,

$$V_{CE} = V_{cc} - R_c * I_c \quad \text{(Equation 1)}$$

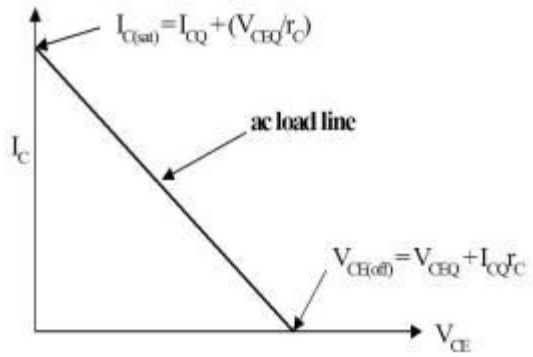
Cutoff point : To find the cutoff point equate the I_c =0, the cutoff point is (V_{cc}, 0).

Saturation point : To find the saturation point equate V_{CE}=0 (actually in saturation the collector voltage will be around o.2 Volts). The saturation point is (0, V_{cc}/R_c).

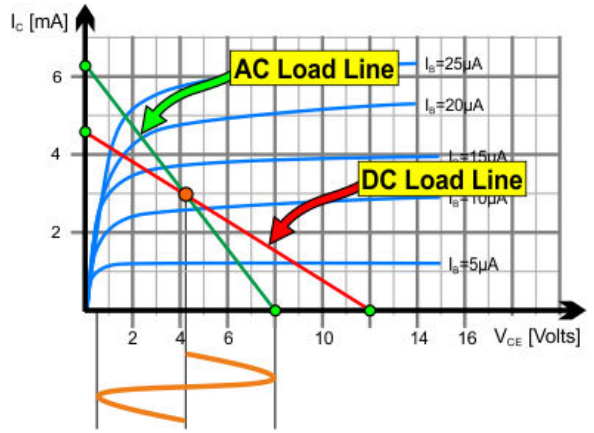
AC load line

DC load line analysis gives the variation of collector currents and voltage for static situation of Zero AC voltage. **The ac load line tells you the maximum possible output voltage swing for a given common-emitter amplifier i.e. the ac load line will tell you the maximum possible peak-to-peak output voltage $V_{ce(cut\ off)}$ from a given amplifier.**

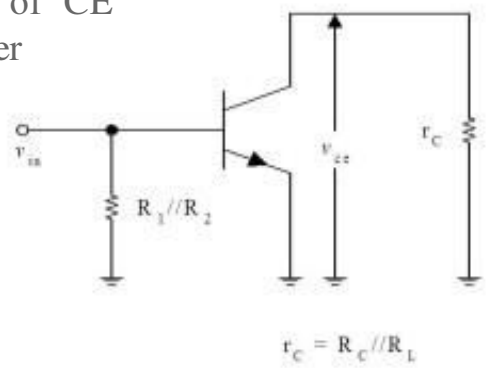
For AC input signal frequencies the biasing capacitors are chosen such that they acts as short circuits and as open circuits for DC voltages. Hence the AC signal equivalent circuit is shown in the figure below along with the AC load line.



AC load line



AC equivalent circuit of CE amplifier



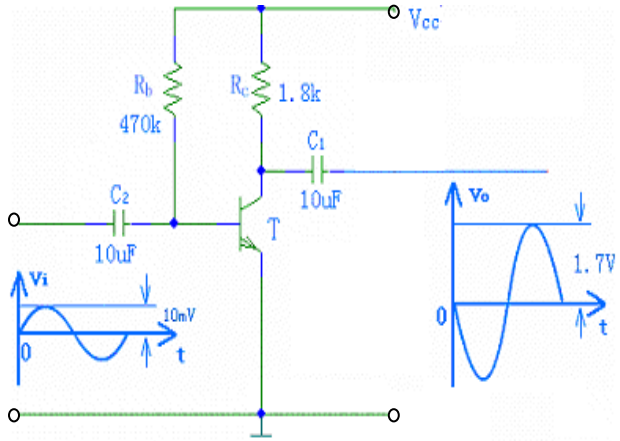
From the AC equivalent circuit we will get $V_{ce} = (R_c//R_L)*I_c$

The AC output V_{ce} can have at most V_{ceq} (since normally the quiescent point is chosen in such a way that the maximum input signal excursion is symmetrical on both negative and positive half cycles i.e $V_{max} = + V_{ceq}$ and $V_{min} = -V_{ceq}$ so that the transistor stays in active region for entire input signal excursion), hence the maximum current for that corresponding V_{ceq} is $V_{ceq} / (R_c//R_l)$. Also output collector current can be at most I_{cq} hence the maximum voltage for that corresponding I_{cq} is $I_{cq}*(R_c//R_l)$. Hence by adding quiescent currents the end points of AC load line are

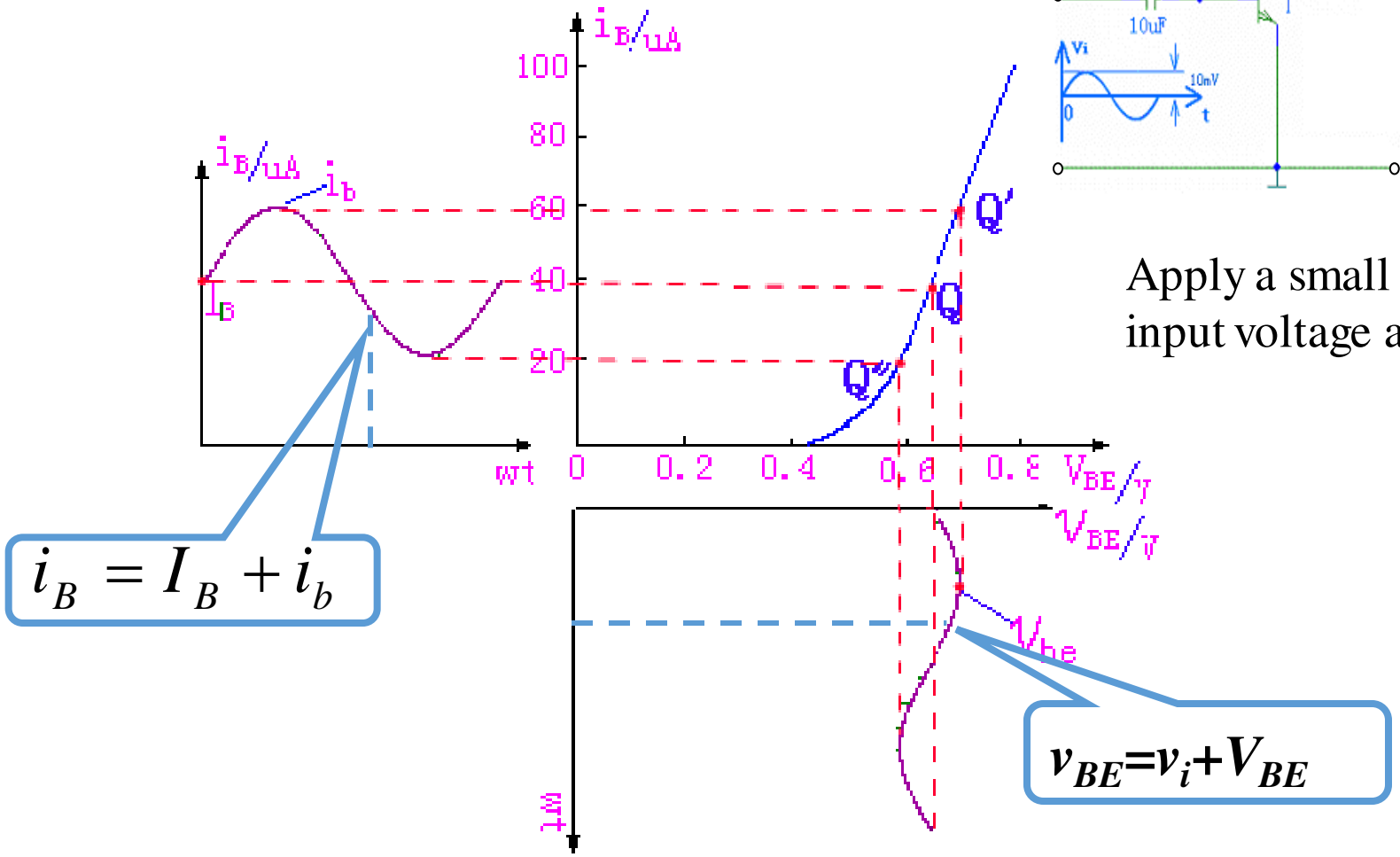
$$I_{c(sa)t} = I_{cq} + V_{ceq}/(R_c//R_l) \text{ and } V_{ce(off)} = V_{ceq} + I_{cq}*(R_c//R_l)$$

Graphical analysis of CE Amplifier

Single-Stage BJT Amplifiers



Apply a small signal input voltage and see i_b

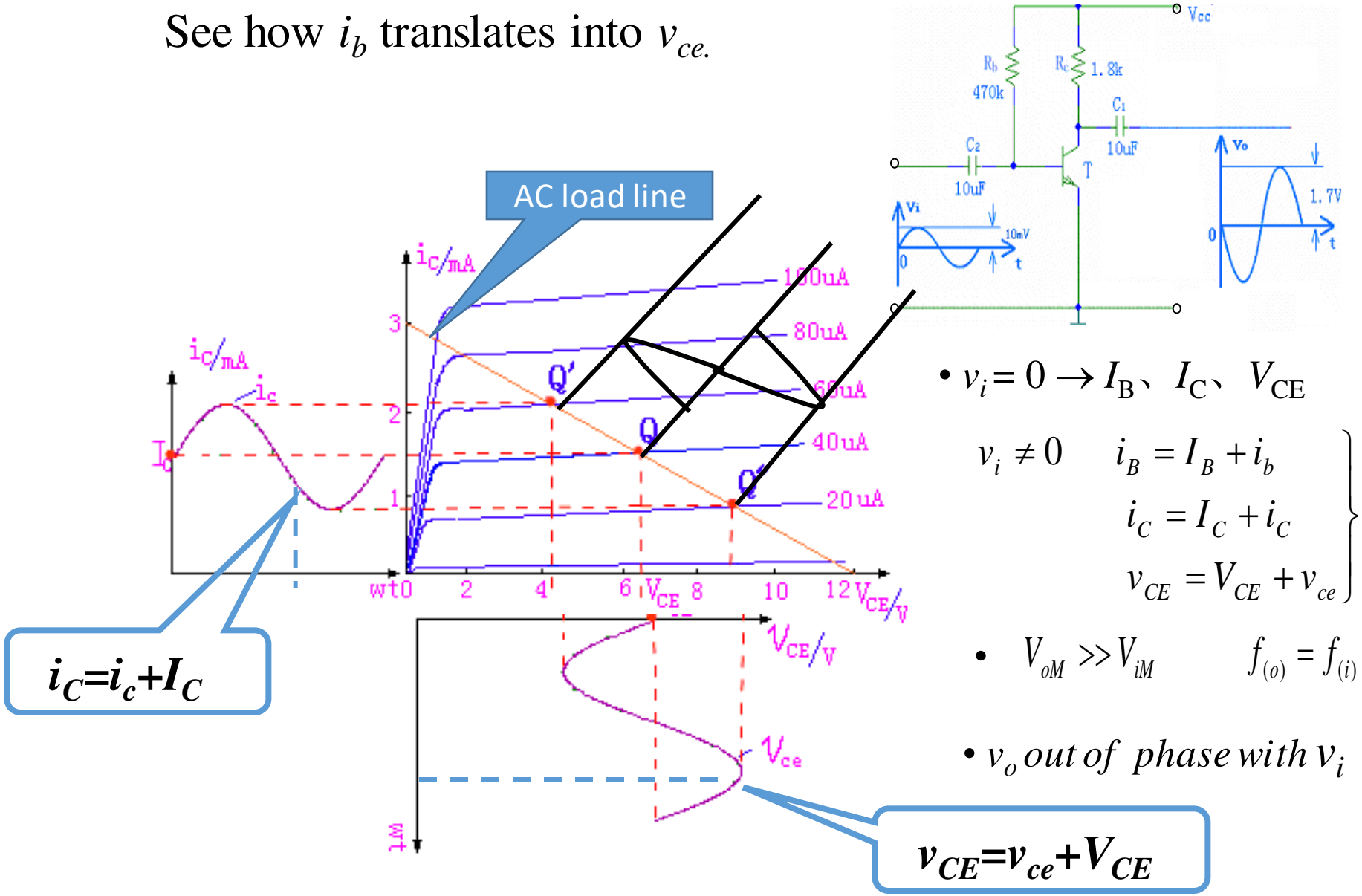


$$i_B = I_B + i_b$$

$$v_{BE}=v_i+V_{BE}$$

Graphical analysis of CE Amplifier

See how i_b translates into v_{ce}.



- $v_i = 0 \rightarrow I_B$、I_C、V_{CE}

$$\left.\begin{array}{ll} v_i \neq 0 & i_B = I_B + i_b \\ & i_C = I_C + i_C \\ & v_{CE} = V_{CE} + v_{ce} \end{array}\right\}$$

- $V_{oM} >> V_{iM}$ $\qquad f_{(o)} = f_{(i)}$

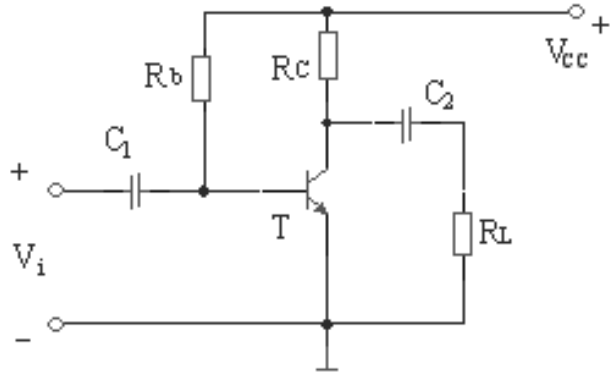
- v_o *out of phase with* v_i

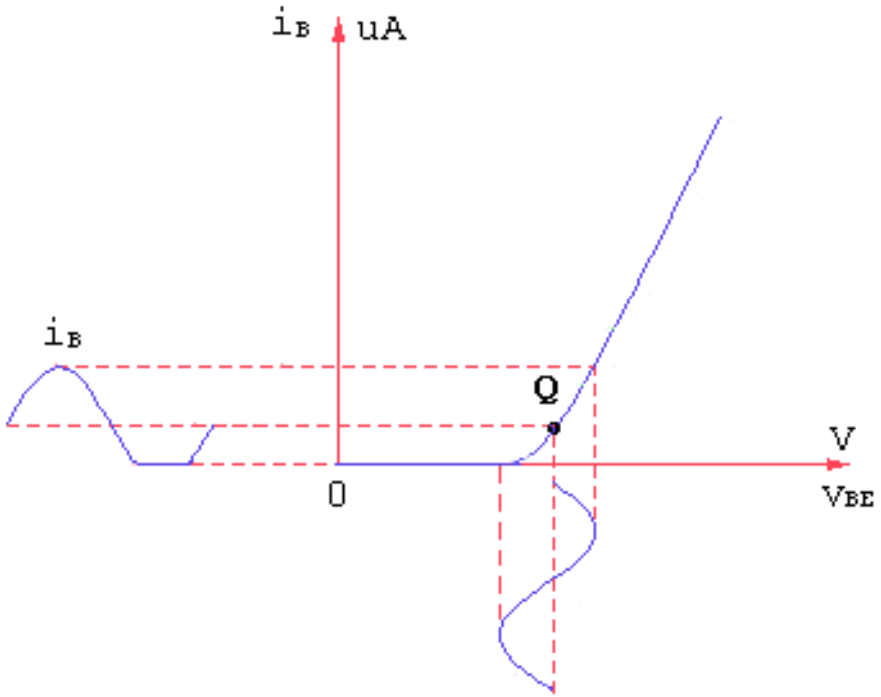
Basic BJT Amplifiers Circuits

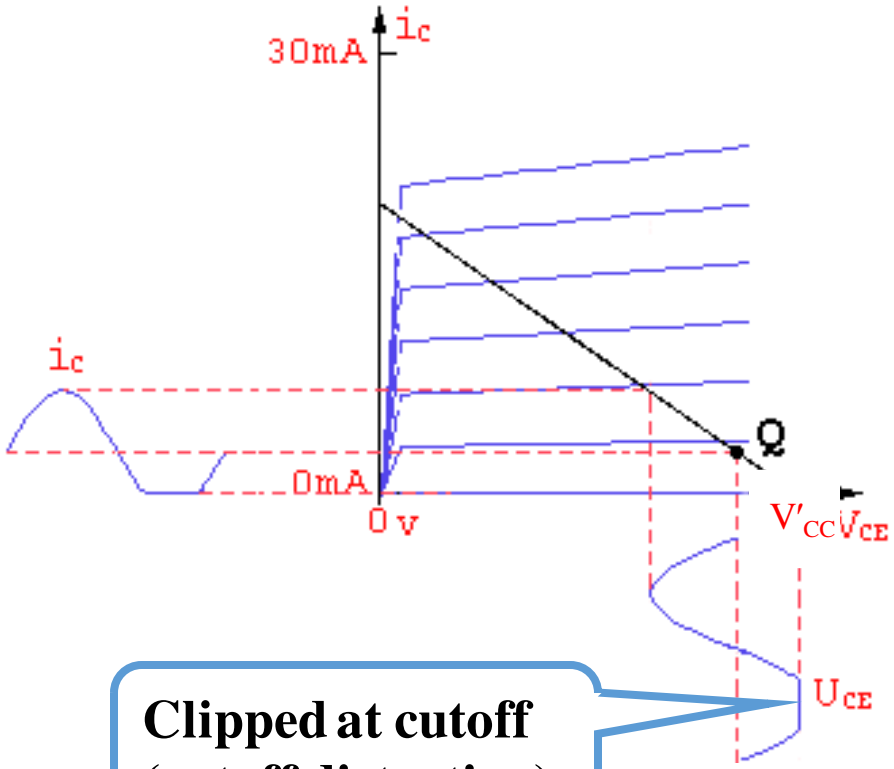
Single-Stage BJT Amplifiers

Graphical Analysis

Q-point closer to cutoff:







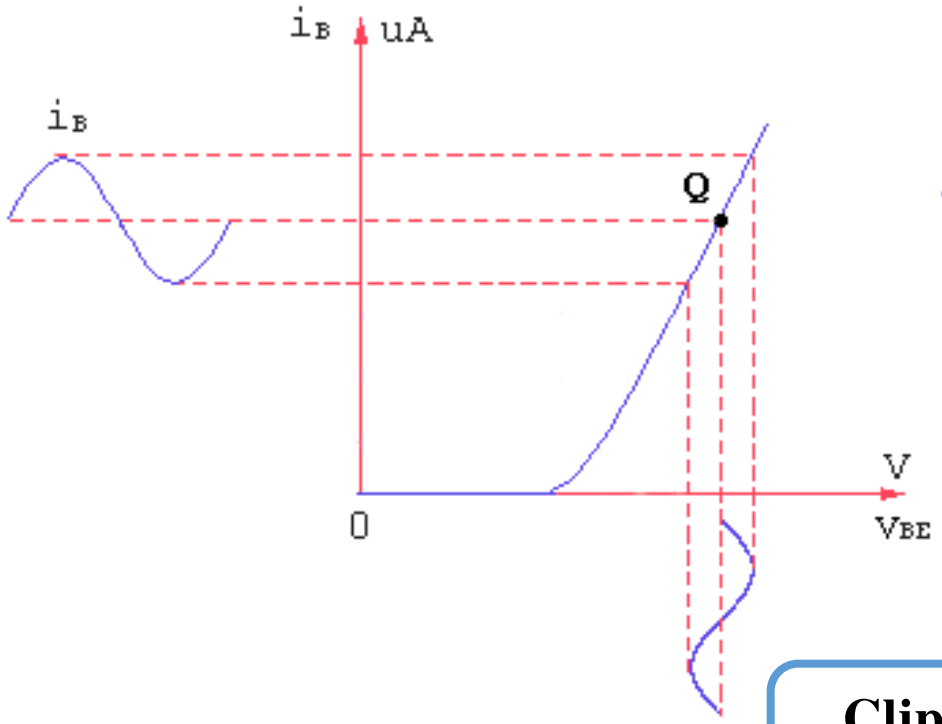
Clipped at cutoff (cutoff distortion)

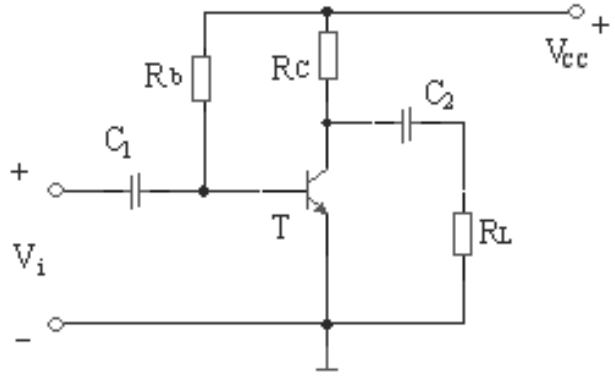
Basic BJT Amplifiers Circuits

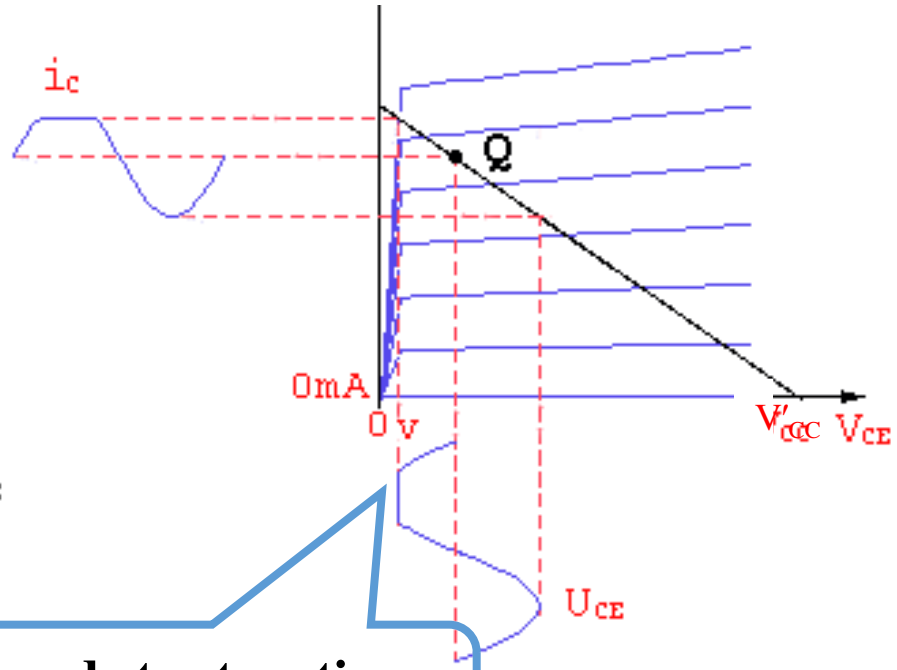
Single-Stage BJT Amplifiers

Graphical Analysis

Q-point closer to saturation:







Clipped at saturation (saturation distortion)

End Lec-2

Transistor Biasing Circuit

Introduction:

It has already been discussed that for faithful amplification, a transistor amplifier must satisfy three basic conditions, namely : (i) proper zero signal collector current, (ii) proper base-emitter voltage at any instant and (iii) proper collector-emitter voltage at any instant.
Transistor Biasing is the fulfilment of these conditions.

Definition: The proper flow of zero signal collector current and the maintenance of proper collector-emitter voltage during the passage of signal is known as **transistor biasing**.
The basic purpose of **transistor biasing** is to keep the base-emitter junction properly forward biased and collector-base junction properly reverse biased during the application of signal.

This can be achieved with a bias battery or associating a circuit with a transistor. The circuit which provides transistor biasing is known as biasing circuit. It may be noted that transistor biasing is very essential for the proper operation of transistor in any circuit.

Inherent Variations of Transistor Parameters

In practice, the transistor parameters such as β, V_{BE} *are not the same for every transistor even of the* same type. To give an example, BC147 is a silicon *npn transistor with β varying from 100 to 600 i.e.* β for one transistor may be 100 and for the other it may be 600, although both of them are *BC147. This,* inherent variations of transistor parameters may change the operating point, resulting in unfaithful amplification.

It is, therefore, very important that *biasing circuit* be so designed that it should be able to work with all transistors of one type whatever may be the spread in β or V_{BE}. *In* other words, the operating point should be independent of transistor parameters variations.

Stabilisation

The collector current in a transistor changes rapidly when
(***i) the temperature changes,***
(***ii) the transistor is replaced by another of the same type. This is due to the inherent variations*** of transistor parameters.

➢When the temperature changes or the transistor is replaced, the operating point (*i.e. zero signal* I_C *and* V_{CE}*) also changes. However, for faithful amplification, it is essential that operating point* remains fixed. This necessitates to make the operating point independent of these variations. This is known as stabilisation.

➢Once stabilisation is done, the zero signal I_C *and* V_{CE} *become independent of temperature variations* or replacement of transistor *i.e. the operating point is fixed.* ***A good biasing circuit always*** **ensures the stabilisation of operating point.**

Need for stabilization

(i) Temperature dependence of I_C

The collector current I_C for CE circuit is given by:

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (\beta + 1) I_{CBO}$$

The collector leakage current I_{CBO} *is greatly influenced (especially in germanium transistor) by temperature* changes. **A rise of 10°C doubles the collector leakage current** which may be as high as 0.2 mA for low powered germanium transistors. As biasing conditions in such transistors are generally so set that zero signal I_C = *1mA, therefore, the change in* I_C *due to temperature variations cannot be tolerated.*

(ii) Individual variations

The value of β and V_{BE} are not exactly the same for any two transistors even of the same type. Further, V_{BE} *itself decreases when temperature increases. When a* transistor is replaced by another of the same type, these variations change the operating point.

(iii) Thermal runaway

The collector current for a CE configuration is given by :

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (\beta + 1) I_{CBO}$$

The collector leakage current I_{CBO} *is strongly dependent on temperature. The flow of collector* current produces heat within the transistor. This raises the transistor temperature and if no stabilisation is done, the collector leakage current I_{CBO} *also increases. It is clear from above eqn. that if* I_{CBO} *increases,* the collector current I_C *increases by* $(\beta + 1)\ I_{CBO}$. *The increased* I_C *will raise the temperature* of the transistor, which in turn will cause I_{CBO} *to increase.*

This effect is cumulative and in a matter of seconds, the collector current may become very large, causing the transistor to burn out. *The self-destruction of an unstabilised transistor is known as* ***thermal runaway.***

In order to avoid thermal runaway and consequent destruction of transistor, it is very essential that operating point is stabilised *i.e.* I_C *is kept constant.*

In practice, this is done by causing I_B ***to*** **decrease automatically with temperature increase by circuit modification.**

Essentials of a Transistor Biasing Circuit

It has already been discussed that transistor biasing is required for faithful amplification.The biasing network associated with the transistor should meet the following requirements :

(i) It should ensure proper zero signal collector current.

(ii) It should ensure that V_{CE} does not fall below 0.5 V for Ge transistors and 1 V for silicon transistors at any instant.

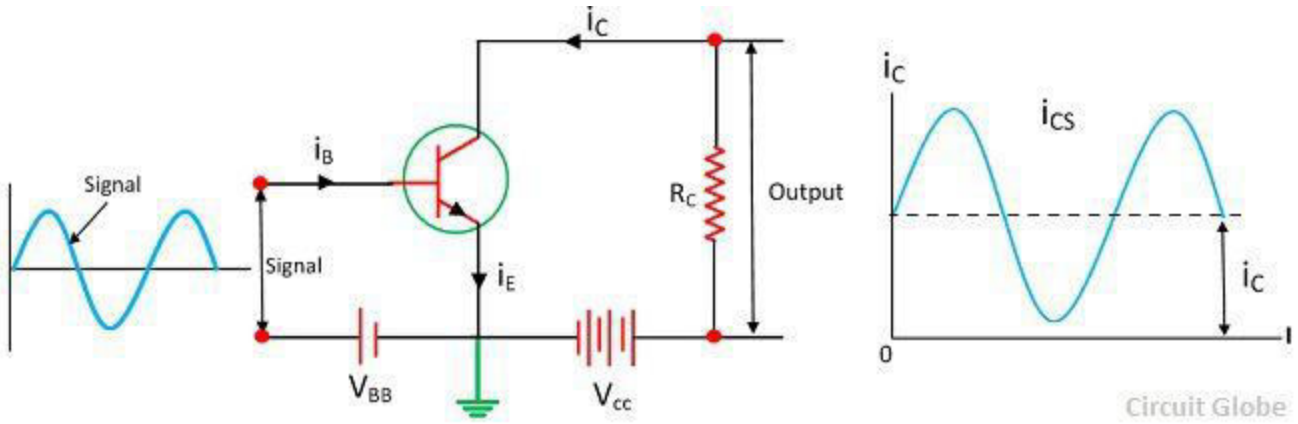
(iii) It should ensure the stabilisation of operating point

Stability Factor

It is desirable and necessary to keep I_C *constant in the face of variations of* I_{CBO} *(sometimes represented* as I_{CO}*). The extent to which a biasing circuit is successful in achieving this goal is measured* by stability factor *S. It is defined as,*
The rate of change of collector current (I_C) *w.r.t. the collector leakage current* (I_{CO}) *at constant* β *and* I_B *is called* ***stability factor i.e.***

$$\text{Stability factor, } S = \frac{dI_C}{dI_{CO}} \text{ at constant } I_B \text{ and } \beta$$

Thus a stability factor 50 of a circuit means that I_C *changes 50 times as much as* any change in I_{CO}. *In order to achieve greater thermal stability, it is desirable to have as low stability* factor as possible.



The general expression of stability factor for a C.E. configuration can be obtained as under:

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

** Differentiating above expression *w.r.t.* I_C, we get,

$$1 = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

or
$$1 = \beta \frac{dI_B}{dI_C} + \frac{(\beta + 1)}{S} \qquad \left[\because \frac{dI_{CO}}{dI_C} = \frac{1}{S}\right]$$

or
$$S = \frac{\beta + 1}{1 - \beta\left(\frac{dI_B}{dI_C}\right)}$$

Methods of Transistor Biasing

In the transistor amplifier circuits drawn so far biasing was done with the aid of a battery V_{BB} *which* was separate from the battery V_{CC} *used in the output circuit. However, in the interest of simplicity* and economy, it is desirable that transistor circuit should have a single source of supply—the one in the output circuit (*i.e.* V_{CC}*). The following are the most commonly used methods of obtaining transistor* biasing from one source of supply (*i.e.* V_{CC} *) :*

***(i) Base resistor method** (fixed-base bias method)*

(ii) Emitter bias method

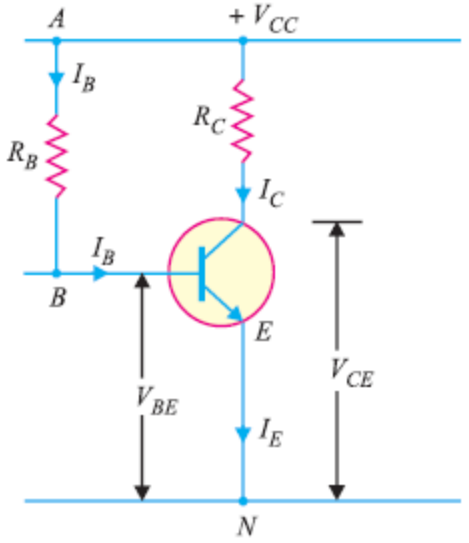
(iii) Biasing with collector-feedback resistor

(iv) Voltage-divider bias

In all these methods, the same basic principle is employed *i.e. required value of base current (and* hence I_C*) is obtained from* V_{CC} *in the zero signal conditions. The value of collector load* R_C *is* selected keeping in view that V_{CE} *should not fall below 0.5 V for germanium transistors and 1 V for* silicon transistors.

Base Resistor Method

In this method, a high resistance R_B *(several hundred kΩ) is* connected between the base and +ve end of supply for *npn* transistor (See Fig) [or between base and negative end of supply for *pnp transistor*]. *Here, the required zero signal* base current is provided by V_{CC} *and it flows through* R_B. Now base is positive *w.r.t. emitter i.e. base-emitter* junction is forward biased. The required value of zero signal base current I_B *(and hence* $I_C = \beta I_B$*) can be made to* flow by selecting the proper value of base resistor R_B.



Circuit analysis. It is required to find the value of R_B so that required collector current flows in the zero signal conditions. Let I_C be the required zero signal collector current.

$$\therefore \quad I_B = \frac{I_C}{\beta}$$

Considering the closed circuit *ABENA* and applying Kirchhoff's voltage law, we get,

$$V_{CC} = I_B R_B + V_{BE} \quad (I_B \text{ do not depend on } I_C)$$

$$\text{or} \quad I_B R_B = V_{CC} - V_{BE}$$

$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} \qquad \ldots (i)$$

As V_{CC} and I_B are known and V_{BE} can be seen from the transistor manual, therefore, value of R_B can be readily found from exp. (i).

Stability factor

In fixed-bias method of biasing, I_B *is independent of* I_C *so that* $dI_B/dI_C = 0$. *Putting the value of* $dI_B/dI_C = 0$ *in,*

$$S = \frac{\beta + 1}{1 - \beta\left(\frac{dI_B}{dI_C}\right)}$$

we have, Stability factor, $S = \beta + 1$, Thus the stability factor in a fixed bias is (β + 1). This means that I_C *changes* $(\beta + 1)$ *times as* much as any change in I_{CO}. *For instance, if* $\beta = 100$, *then* $S = 101$ *which means that IC increases 101* times faster than *ICO. Due to the large value of S in a fixed bias, it has poor thermal stability.*

Advantages :

(i) This biasing circuit is very simple as only one resistance R_B ***is required.***

(ii) Biasing conditions can easily be set and the calculations are simple.

(iii) There is no loading of the source by the biasing circuit since no resistor is employed across base-emitter junction.

Disadvantages :

(i) This method provides poor stabilisation. It is because there is no means to stop a self-increase in collector current due to temperature rise and individual variations. For example, if β increases due to transistor replacement, then I_C *also increases by the same factor as* I_B *is constant.*

(ii) The stability factor is very high. Therefore, there are strong chances of thermal runaway.

Due to these disadvantages, this method of biasing is rarely employed.

Emitter Bias Circuit

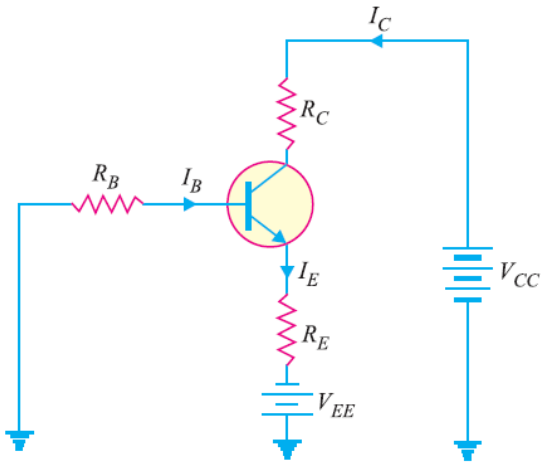


Fig. shows the emitter bias circuit. This circuit differs from base-bias circuit in two important respects. First, it uses two separate d.c. voltage sources ; one positive ($+V_{CC}$) *and the other negative* ($-V_{EE}$). *Normally, the two supply voltages will be equal. For example, if* V_{CC}= +20V *(d.c.), then* V_{EE}= – 20V (d.c.). Secondly, there is a resistor R_E *in the emitter circuit.*

Circuit analysis:

(*i*) Collector current (I_C). Applying Kirchhoff's voltage law to the base-emitter circuit in Fig. 9.16, we have,

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$\therefore \quad V_{EE} = I_B R_B + V_{BE} + I_E R_E$$

Now $I_C \simeq I_E$ and $I_C = \beta I_B \quad \therefore I_B \simeq \dfrac{I_E}{\beta}$

Putting $I_B = I_E/\beta$ in the above equation, we have,

$$V_{EE} = \left(\frac{I_E}{\beta}\right) R_B + I_E R_E + V_{BE}$$

or $$V_{EE} - V_{BE} = I_E (R_B/\beta + R_E)$$

$$\therefore \quad I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

Since $I_C \simeq I_E$, we have,

$$I_C = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

Applying Kirchhoff's voltage law to the collector side of the emitter bias circuit in Fig. 9.16 (Refer back), we have,

$$V_{CC} - I_C R_C - V_{CE} - I_C^* R_E + V_{EE} = 0$$

or $$V_{CE} = V_{CC} + V_{EE} - I_C (R_C + R_E)$$

Stability of Emitter bias. The expression for collector current I_C for the emitter bias circuit is given by ;

$$I_C \simeq I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B / \beta}$$

It is clear that I_C is dependent on V_{BE} and β, both of which change with temperature.

If $R_E >> R_B/\beta$, then expression for I_C becomes :

$$I_C = \frac{V_{EE} - V_{BE}}{R_E}$$

This condition makes $I_C (\simeq I_E)$ independent of β.

If $V_{EE} >> V_{BE}$, then I_C becomes :

$$I_C (\simeq I_E) = \frac{V_{EE}}{R_E}$$

This condition makes $I_C (\simeq I_E)$ independent of V_{BE}.

If $I_C (\simeq I_E)$ is independent of β and V_{BE}, the Q-point is not affected appreciably by the variations in these parameters. Thus emitter bias can provide stable Q-point if properly designed.

End of Lec-3